8086 Bus Cycle and Timing Diagram

The BIU initiates all external operations which are also called bus activity. The

external bus activities are repetitions of certain basic operations. The basic

operations performed by the CPU bus are called bus cycles. Depending on the

activities of 8086 ,the bus cycles can be classified as

● Memory read cycle

● Memory write cycle

● I/O read cycle

● I/O write cycle

● Interrupt acknowledge cycle

The processor takes a definite time to perform a bus cycle. The time taken to

perform a bus cycle is specified in terms of term T- states. In 8086 processor the

time duration of one T-state is equal to one time period of the interval clock of the

processor.

Timing diagram provides information about the various conditions ( high state or low

state)of the signals while a bus cycle is executed. **Timing diagram is a graphical**

**representation of the operations of microprocessor with respect to time.**

**State: one cycle of the clock is called state.**

**Machine cycle: The basic microprocessor operation such as reading a byte from**

**memory or writing a byte** to a port is called machine cycle and made up of more than

one state.

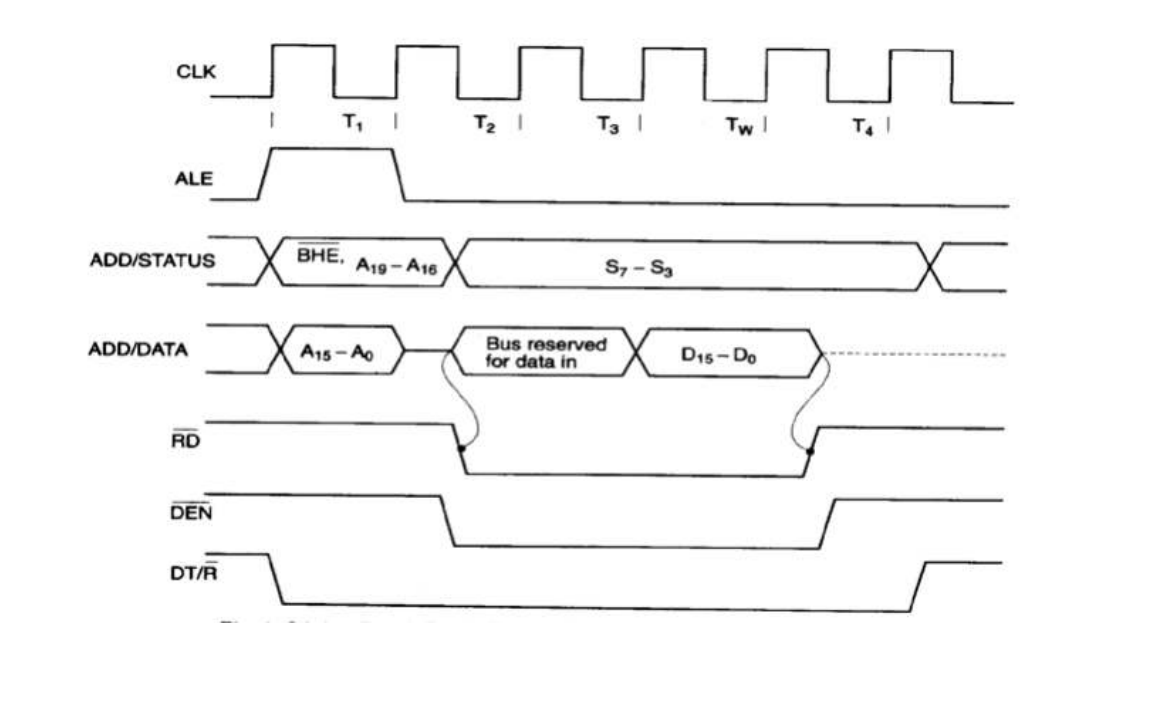
**Instruction cycle: The time required for a microprocessor to fetch and execute an**

**entire instruction is called Instruction cycle and made up of more than one machine**

**cycle.**

**An instruction cycle is made up of machine cycles, and a machine cycle is made up**

**of states.** The time for a state is determined by the frequency of the clock signal.

Read cycle timing diagram for Minimum mode

The best way to analyze a timing diagram such as the one to think of time as a

vertical line moving from left to right across the diagram.

● The read cycle begins in T1 with the assertion of the address latch enable

(ALE) signal and also M/IO’ signal.

● During the negative going edge of this signal, the valid address is latched on

the local bus. The BHE’ and A0 signals address low, high or both bytes.

● From T1 to T4, the M/IO’ signal indicate a memory or I/O operation. At T2, the

address is removed from the local bus and is sent to the output. The bus is

then tristated. The read (RD ) control signal is also activated in T2.

● The read (RD ) signal causes the addressed device to enable its data bus

drivers. After RD goes low, the valid data is available on the data bus. The

addressed device will drive the READY line high. When the processor returns

the read signal to high level, the addressed device will again tristate its bus

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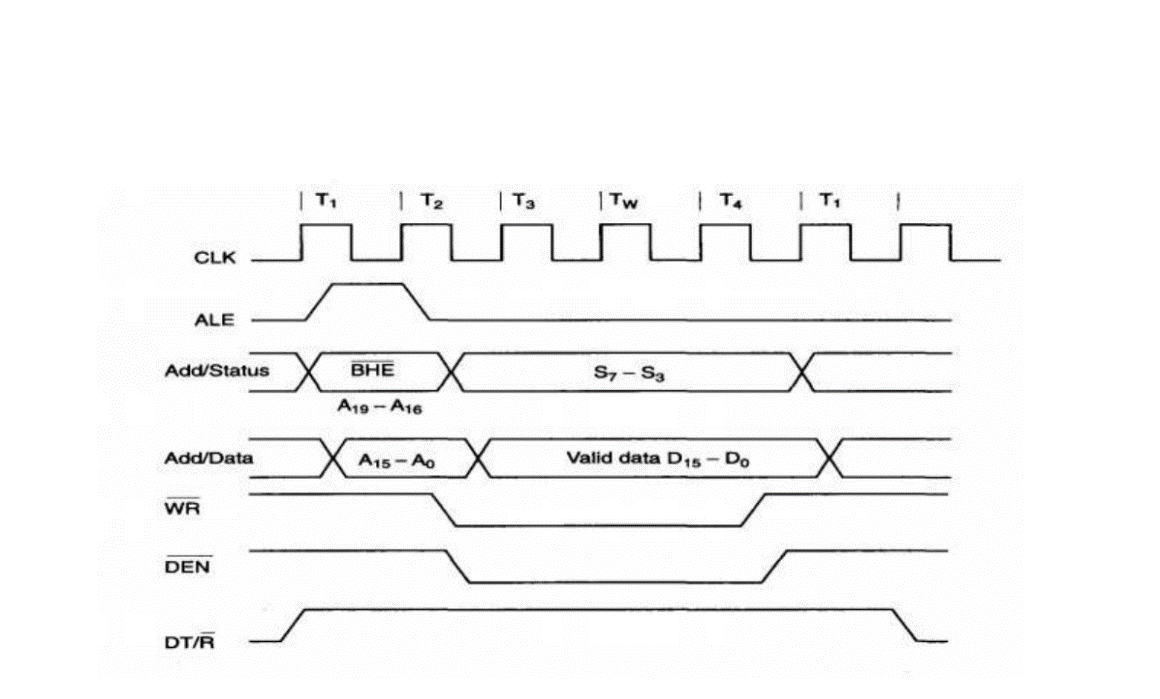
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Write cycle timing diagram for Minimum mode



A write cycle also begins with the assertion of ALE and the emission of the

address. The M/IO’ signal is again asserted to indicate a memory or I/O

operation.

● In T2, after sending the address in T1, the processor sends the data to be

written to the addressed location. The data remains on the bus until the middle

of T4 state. The WR’ becomes active at the beginning of T2 (unlike RD’ is

somewhat delayed in T2 to provide time for floating).

● The BHE’ and A0 signals are used to select the proper byte or bytes of

memory or I/O word to be read or written.

● The M/IO’, RD’ and WR’ signals indicate the types of data transfer as specified

in Table

